# Pax wang

Technology Development Director, UMC

## Rewiring Edge AI System Efficiency with Advanced Packaging

The rapid deployment of AI across both data centers and edge devices is driving unprecedented demand for high bandwidth, compute density, and energy efficiency. Edge AI applications, from autonomous vehicles to mobile, wearables and smart industrial systems, increasingly require localized inference capabilities, and therefore pushing packaging technologies to evolve beyond traditional boundaries.

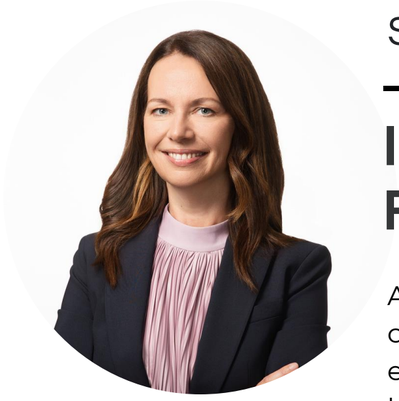
This presentation explores the key trends in advanced packaging, including the evolution of interposer technology, emerging edge use cases for hybrid bonding, and power delivery integration. With node scaling prohibitively expensive for the majority of edge use cases, hybrid bonding in particular will play a key role in enabling innovative package configurations with mature node processes. In addition to technical aspects, collaborative and integration-ready solutions will also be key in driving heterogeneous integration in the AI era.

## Biography

Pax Wang is currently the Technology Development Director of the Advanced Packaging Division at UMC, where he leads the strategic development of advanced packaging technologies, including 2.5D and 3D advanced packaging solutions. Since joining UMC in 2013, he has played a pivotal role in delivering key technology development projects, such as 14nm FinFET and 28nm eNVM. Prior to UMC, Pax worked at TSMC from 2010 to 2013, focusing on advanced FinFET platforms.

With over a decade of extensive experience in FEOL integration R&D and system-level marketing, and holding over 100 patents, Pax bridges front-end innovation with back-end packaging solutions to meet the evolving demands of AI and heterogeneous computing.

# Audrey Charles



Senior Vice President of Corporate Strategy and Advanced Packaging; President of Lam Capital

## Interconnect Horizons: Wafer and Panel Innovation and Industry Partnerships to Unlock AI's Next Leap

As AI systems scale in complexity and capability, their demands for bandwidth, power efficiency, and heterogeneous integration are rapidly outpacing the capabilities of today's packaging interconnect solutions. The industry faces a critical inflection point: wafer- and panel-level integration platforms must evolve to overcome mounting challenges in thermal management, signal integrity, and yield—especially as extra-large die and chiplet architectures become the norm.

This keynote will explore the frontier of heterogeneous integration and its pivotal role in enabling the next generation of AI hardware. We will examine emerging interconnect architectures on both wafer and panel format designed to break through current limitations, with a focus on chiplet-photonics-memory co-packaging and the enabling materials and process innovations required to support them.

Crucially, in the keynote, we shall advocate for an open, collaborative ecosystem—one that fosters healthy competition, accelerates co-innovation in materials science, and aligns around shared platforms to drive scalable progress. Only through collective industry action can we dismantle the "integration wall" and unlock AI's next leap.

## Biography

Audrey Charles is senior vice president of corporate strategy and advanced packaging, and president of Lam Capital at Lam Research. In this position, she is responsible for leading the executive management team in the development of strategic priorities and key initiatives that support the company's long-term profitable growth. She is also responsible for accelerating the company's market-leading position in advanced packaging to deliver differentiated technology and support to customers.

Additionally, Audrey oversees Lam's Corporate Development team and investment arm, Lam Capital, which invests in disruptive companies that advance the semiconductor ecosystem through next generation industrial automation, technology and product innovation, and new market opportunities. She brings a broad base of experience to her role, including engineering, customer technology management and investor relations. Since joining Lam in 1995, she has served in a range of leadership positions including senior vice president of Global Human Resources and vice president of corporate initiatives. Audrey earned an M.B.A. from the MIT Sloan School of Management and a B.S. in applied physics from Dublin City University.

# Radha Nagarajan

Senior Vice President and Chief Technology Officer, Marvell's Optical Engineering Group

## Scaling AI Infrastructure with Advanced Optical Interconnects

Low power, highly integrated optical interconnects are critical as the AI infrastructures exponentially scale to million XPU clusters. At the core, heterogeneous integration of CMOS, SiGe and Photonics of various flavors is needed to realize the small, power efficient light engines needed to implement the massive optical interconnect network. We discuss the role of advanced packaging in enabling such an AI driven infrastructure growth.

## Biography

Dr. Nagarajan is currently the Senior Vice President and Chief Technology Officer of Marvell's Optical Engineering Group . At Marvell, he manages the development of the company's optical platform products and technology. Concurrently, he is a Visiting Professor at the Department of Electrical and Computer Engineering at the National University of Singapore. He received his B.Eng. from NUS, M.Eng. from the University of Tokyo, and Ph.D. from the University of California, Santa Barbara, all in Electrical Engineering.
Dr. Nagarajan has been elected to the National Academy of Engineering (US). His other recognitions include the IEEE/LEOS Aron Kressel Award, the IPRM Award and the Optica David Richardson Medal for breakthrough work in the development and manufacturing of photonic integrated circuits. He has been awarded more than 250 US patents and is a Fellow of the IEEE, Optica, and IET.

# Prof. Dr. Harald Kuhn

Director, Fraunhofer Institute for Electronic Nano Systems ENAS

## Driving Innovation Through Hetero-Integration: Technologies, Challenges and Future Directions

The rapid evolution of semiconductor technology confronts the industry with fundamental challenges:The limits of classic scaling are being reached, and the future of high-performance electronics lies in Hetero-Integration – the strategic combination of diverse components into a single, complex 3D system. This presentation highlights the decisive technologies, the associated challenges, and the future directions we must pursue to drive innovation in micro-assembly. At the heart of this new era are the Advanced Wafer Bonding Technologies. They are the central element in the fabrication of heterogeneously integrated systems and demands precision at the atomic level. We will examine the complexities and latest advancements in the Wafer-to-Wafer and Die-to-Wafer bonding techniques and illuminate their critical function, particularly using the example of Chemical Mechanical Planarization (CMP), which is the essential step also for Hybrid Bonding.

This new alternative to micro-bumping bonding approaches is currently under development also for various Power Electronics applications including those with WBG Devices as part of heterogeneous systems. The latest developments and their direct impact on the performance and integration density of future semiconductor devices will be analyzed in detail – with the special focus on European applications such as automotive, industrial, and infrastructural products and their use in harsh environment and safety critical contexts.